AMENDMENTS TO THE DRAWINGS

The attached sheet(s) of drawings include changes to Fig. 4 and new Fig. 5 replaces the original sheet(s) including such figures.

Attachment(s): Replacement Sheet including amended Fig. 4 and new Fig. 5; and
Annotated Sheet Showing Changes to amended Fig. 4.

REMARKS

This paper is responsive to the Non-Final Office Action dated August 26, 2004. Claims 1-28 were examined. The drawings are objected to under 37 C.F.R. § 1.83(a). Claims 9, 16-18, 25, and 26 are objected to under 35 U.S.C. § 112, second paragraph. Claims 1-11, 13-15, 18-20, and 23-28 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,707,318 to Kumar et al. Claims 12, 21, and 22 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kumar in view of U.S. Patent No. 6,542,006 to Sprague et al.

Objections to the Drawings

The drawings are objected to under 37 C.F.R. § 1.83(a) for failing to show every feature of the invention specified in the claims. Figure 4 has been amended to indicate that weak keeper 420 is a weak keeper. This amendment is supported at least in the specification at page 6, paragraph 1022. No new matter is added. In addition, Figure 4 was amended to clarify the connections between pull-down devices 206 and 208 to dynamic node 216 and to clarify the connection between weak keeper 420 to dynamic node 216. Figure 5 has been added to illustrate that the dynamic node is precharged low and the evaluation circuit is p-logic. Figure 5 is supported at least by paragraph [1026] in the specification as filed on June 27, 2003 and originally filed claims 21 and 22. No new matter is added.

Amendments to the Specification

The specification has been amended to refer to Figure 5 and to correct typographical errors. No new matter is added.

Claim Objections Under 35 U.S.C. § 112, second paragraph

Claims 9, 16-18, 25, and 26 stand objected to under 35 U.S.C. § 112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. The Office Action states that "[t]he term 'weak keeper device' in claims 9, 18, and 26 is a relative term, which renders the claim indefinite." Applicants respectfully maintain that one of ordinary skill in the art would understand the term "weak keeper device" in light of the specification. See, for example, the specification beginning at page 1, paragraph [1003], line 3, which recites that "[k]eeper 112 is a weak keeper, that is, a p-

transistor designed to have a low gain achieved by a small W/L ratio so that the gain is low enough to be overcome by pull-down transistors 104-110."

Claim 16 has been amended to recite "an earliest signal transitioning to a level that can discharge the dynamic node."

Claim 17 has been amended to recite "a latest signal transitioning to a level that can discharge the dynamic node."

Claim 25 has been amended to recite "a keeper device."

Claim Rejections Under 35 U.S.C. § 102(e)

Claims 1-11, 13-15, 18-20, and 23-28 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Kumar. Claim 1 has been amended to recite that

> the effective strength of the keeper circuit operating on the dynamic node is reduced from a first non-zero strength level to a second non-zero strength level during an interval in which at least one path in an evaluation circuit is sensitive to a keeper device.

Regarding amended claim 1, Applicants respectfully maintain that Kumar, alone or in combination with other references of record, fails to teach or suggest that

> reducing from a first non-zero strength level to a second non-zero strength level during an interval in which at least one path in an evaluation circuit is sensitive to a keeper device,

as required by amended claim 1. Kumar teaches a keeper circuit that during a precharge phase of the clock, neither nMOSFET 316 nor pMOSFET 314 are enabled and the keeper circuit is not operating on node 308. (Col. 2, lines 46-52) During an evaluation phase of Kumar, a clock signal ϕ is enabled by pass nMOSFET 311. (Col. 2, lines 54-57) Depending upon the impedance path between node 308 and ground, either nMOSFET 316 or pMOSFET 314 of

Kumar is on to maintain a LOW value on node 308 or to maintain a HIGH value on node 308, respectively. (Col. 2, lines 59-64) However, Kumar introduces a signal delay by inverter 312 and pass nMOSFET 311 such that pMOSFET 314 is disabled at the beginning of an evaluation phase. (Col. 3, lines 11-14) Note that at the beginning of an evaluation phase of Kumar, nMOSFET 316 is also disabled due to the DYNAMIC OUT being LOW during the precharge phase. (Col. 2, lines 50-52) Thus, at the beginning of Kumar's evaluation phase, neither pMOSFET 314 nor nMOSFET 316 is enabled and the keeper circuit is not operating on node 308. During the remainder of Kumar's evaluation phase, either pMOSFET 314 or nMOSFET 316 is pulling down or pulling up node 308. Nowhere does Kumar teach or suggest a keeper circuit having a first and a second non-zero strength level. For this reason, Applicants respectfully maintain that amended claim 1 distinguishes over Kumar and all references of record. Accordingly, Applicants respectfully request that the rejection of claim 1 and all claims dependent thereon, be withdrawn.

Claim 4 has been cancelled.

Claim 5 has been amended to recite

> a keeper circuit coupled to the dynamic node, wherein the keeper circuit has a first non-zero strength during a first interval and a second non-zero strength during a second interval, the first non-zero strength being substantially greater than the second non-zero strength

Regarding amended claim 5, Applicants respectfully maintain that Kumar, alone or in combination with other references of record, fails to teach or suggest

> a keeper circuit having a first non-zero strength during a first interval and a second non-zero strength during a second interval

as required by amended claim 5. Kumar teaches a keeper circuit that during a precharge phase of the clock, neither nMOSFET 316 nor pMOSFET 314 are enabled and the keeper circuit is not

operating on node 308. (Col. 2, lines 46-52) During an evaluation phase of Kumar, a clock signal ϕ is enabled by pass nMOSFET 311. (Col. 2, lines 54-57) Depending upon the impedance path between node 308 and ground, either nMOSFET 316 or pMOSFET 314 of Kumar is on to maintain a LOW value on node 308 or to maintain a HIGH value on node 308, respectively. (Col. 2, lines 59-64) However, Kumar introduces a signal delay by inverter 312 and pass nMOSFET 311 such that pMOSFET 314 is disabled at the beginning of an evaluation phase. (Col. 3, lines 11-14) Note that at the beginning of an evaluation phase of Kumar, nMOSFET 316 is also disabled due to the DYNAMIC OUT being LOW during the precharge phase. (Col. 2, lines 50-52) Thus, at the beginning of Kumar's evaluation phase, neither pMOSFET 314 nor nMOSFET 316 is enabled and the keeper circuit is not operating on node 308. During the remainder of Kumar's evaluation phase, either pMOSFET 314 or nMOSFET 316 is pulling down or pulling up node 308. Nowhere does Kumar teach or suggest a keeper circuit having a first non-zero strength during a first interval and a second non-zero strength during a second interval. For this reason, Applicants respectfully maintain that amended claim 5 distinguishes over Kumar and all references of record. Accordingly, Applicants respectfully request that the rejection of claim 5 and all claims dependent thereon, be withdrawn.

Claim 7 is amended to provide antecedent basis consistent with amendments to claim 5.

Claims 8, 9, 13, are amended to clarify the invention.

Claim 15 is amended to depend from claim 7.

Claim 23 is amended to recite

`protecting the dynamic node from noise during the interval.`

Regarding amended claim 23, Applicants respectfully maintain that Kumar, alone or in combination with other references of record, fails to teach or suggest a keeper circuit that effectively disables a keeper device coupled to a dynamic node during an interval in which at least one path in an evaluation circuit is sensitive to the keeper device and protecting the dynamic node from noise during the interval, as required by amended claim 23. For this reason, Applicants respectfully maintain that amended claim 23 distinguishes over Kumar and all

references of record. Accordingly, Applicants respectfully request that the rejection of claim 23 be withdrawn.

Claims 24 is cancelled.

Claim 25 is amended to recite

> reducing effective keeper circuit strength from a first non-zero strength to a second non-zero strength during an interval in which at least one path of an evaluation circuit is sensitive to a keeper device.

Regarding amended claim 25, Applicants respectfully maintain that Kumar, alone or in combination with other references of record, fails to teach or suggest

> reducing effective keeper circuit strength from a first non-zero strength to a second non-zero strength during an interval in which at least one path of an evaluation circuit is sensitive to a keeper device,

as required by amended claim 25. Kumar teaches a keeper circuit that during a precharge phase of the clock, neither nMOSFET 316 nor pMOSFET 314 are enabled and the keeper circuit is not operating on node 308. (Col. 2, lines 46-52) During an evaluation phase of Kumar, a clock signal ϕ is enabled by pass nMOSFET 311. (Col. 2, lines 54-57) Depending upon the impedance path between node 308 and ground, either nMOSFET 316 or pMOSFET 314 of Kumar is on to maintain a LOW value on node 308 or to maintain a HIGH value on node 308, respectively. (Col. 2, lines 59-64) However, Kumar introduces a signal delay by inverter 312 and pass nMOSFET 311 such that pMOSFET 314 is disabled at the beginning of an evaluation phase. (Col. 3, lines 11-14) Note that at the beginning of an evaluation phase of Kumar, nMOSFET 316 is also disabled due to the DYNAMIC OUT being LOW during the precharge phase. (Col. 2, lines 50-52) Thus, at the beginning of Kumar's evaluation phase, neither pMOSFET 314 nor nMOSFET 316 is enabled and the keeper circuit is not operating on node 308. During the remainder of Kumar's evaluation phase, either pMOSFET 314 or nMOSFET 316 is pulling down or pulling up node 308. Nowhere does Kumar teach or suggest reducing effective keeper

circuit strength from a first non-zero strength to a second non-zero strength during an interval in which at least one path of an evaluation circuit is sensitive to a keeper device. For this reason, Applicants respectfully maintain that amended claim 25 distinguishes over Kumar and all references of record. Accordingly, Applicants respectfully request that the rejection of claim 25 and all claims dependent thereon, be withdrawn.

Claim 27 is amended to recite

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a dynamic node, a first keeper device coupled to the
dynamic node, and means for protecting the dynamic
node from noise during the interval.
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Regarding amended claim 27, Applicants respectfully maintain that Kumar, alone or in combination with other references of record, fails to teach or suggest

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means for protecting the dynamic node from noise
during the interval,
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as recited by amended claim 27. Kumar teaches a keeper circuit that during a precharge phase of the clock, neither nMOSFET 316 nor pMOSFET 314 are enabled and the keeper circuit is not operating on node 308. (Col. 2, lines 46-52) During an evaluation phase of Kumar, a clock signal ϕ is enabled by pass nMOSFET 311. (Col. 2, lines 54-57) Depending upon the impedance path between node 308 and ground, either nMOSFET 316 or pMOSFET 314 of Kumar is on to maintain a LOW value on node 308 or to maintain a HIGH value on node 308, respectively. (Col. 2, lines 59-64) However, Kumar introduces a signal delay by inverter 312 and pass nMOSFET 311 such that pMOSFET 314 is disabled at the beginning of an evaluation phase. (Col. 3, lines 11-14) Note that at the beginning of an evaluation phase of Kumar, nMOSFET 316 is also disabled due to the DYNAMIC OUT being LOW during the precharge phase. (Col. 2, lines 50-52) Thus, at the beginning of Kumar's evaluation phase, neither pMOSFET 314 nor nMOSFET 316 is enabled and the keeper circuit is not operating on node 308. During the remainder of Kumar's evaluation phase, either pMOSFET 314 or nMOSFET 316 is pulling down or pulling up node 308. Nowhere does Kumar teach or suggest means for protecting the dynamic node from noise during the interval. For this reason, Applicants respectfully maintain that amended claim 27 distinguishes over Kumar and all references of record. Accordingly,

Applicants respectfully request that the rejection of claim 27 and all claims dependent thereon, be withdrawn.

Claim 28 is cancelled.

New claims 29-36 are added. Applicants believe that new claims 29-36 distinguish over the art of record.

Claim Rejections Under 35 U.S.C. § 103(a)

Claims 12, 21, and 22 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kumar in view of U.S. Patent No. 6,542,006 to Sprague et al. Applicants believe claims 12, 21, and 22 depend from allowable claims and are allowable for at least this reason. Accordingly, Applicants respectfully request that the rejection of these claims and all claims dependent thereon, be withdrawn.

In summary, claims 1-3, 5-23, 25-27, and 29-36 are in the case. All claims are believed to be allowable over the art of record, and a Notice of Allowance to that effect is respectfully solicited. Nonetheless, if any issues remain that could be more efficiently handled by telephone, the Examiner is requested to call the undersigned at the number listed below.

CERTIFICATE OF MAILING OR TRANSMISSION

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Date

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Respectfully submitted,

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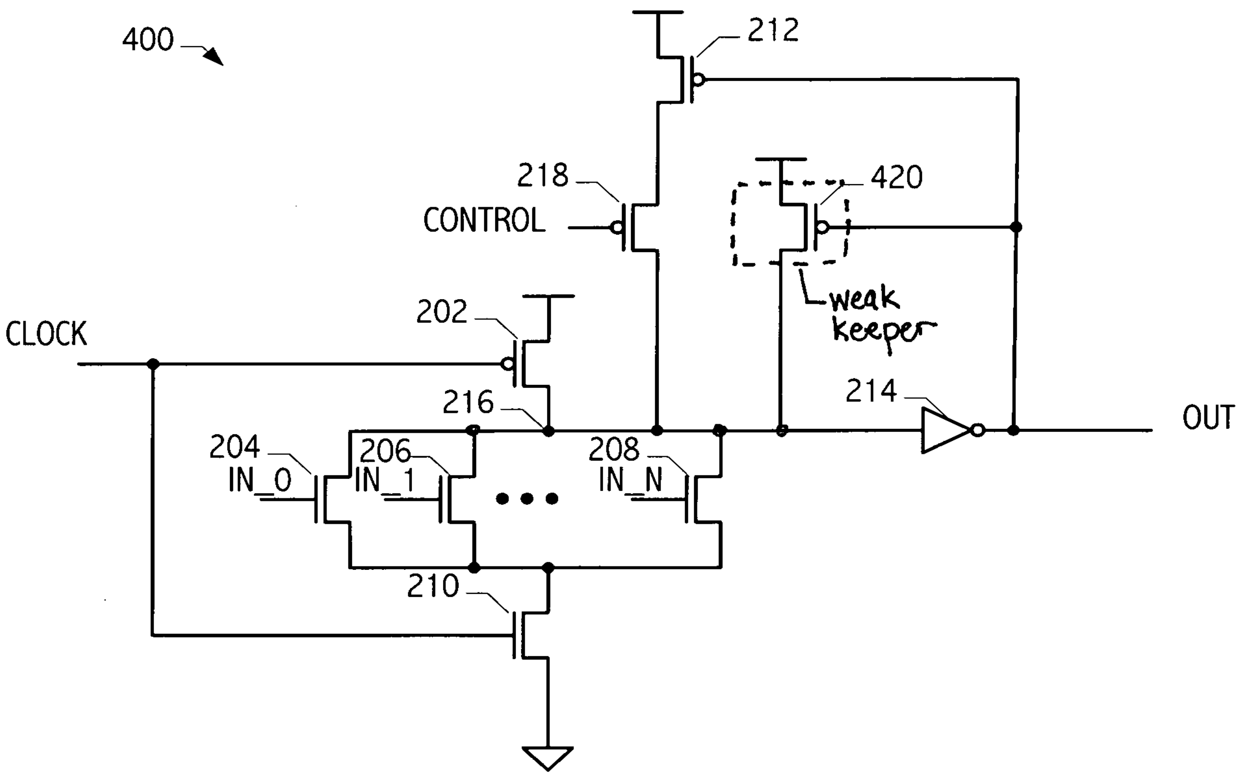

FIG. 4